ROHM SEMICONDUCTOR

Electronics for the Future

【Additional approval and change approval document】

Affected Manufacturing Department: HPD Division
Affected product group: SiC

SiC 6-inch factory additional approval

Document ID:2222002_PCN Details

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1. Background of the change

[About SiC 6inch additional approval]

In order to expand the production capacity , we are planning to introduce larger wafer sizes ,

6inch instead of 4inch.

For the future supply , We ask for your cooperation to approve.

*Wafer manufacturing plants of new products have proven track records with SiC 4GMOSFET and other Si products.

For the 4-inch line, production is scheduled to end after the 6-inch line transition.

2. Summary of this approval

Scope	SiC 3rd Generation MOSFET TO-247N Package
Content	With regard to the above products, we will expand the wafer manufacturing process from the current ROHM Apollo Co., Ltd. Chikugo Plant to the Miyazaki Plant of Lapis Semiconductor Co., Ltd. The specifications and performance of the final product, including electrical characteristics and reliability, are unchanged.
Reason	To expand production capacity
Verification	1. Verification of changes between current and additional plants. 2. Comparison of specifications and performance between current products and new products.
Schedule	Please respond within one year after receipt of the application.

3.Summary of changes

PCN No.2222002

Fabrication (Wafer manufacturing)

	Using	Change Request
Factory	ROHM Apollo co., ltd. (Chikugo)	LAPIS Semiconductor Co., Ltd. (Miyazaki)
SiC Wafers	4 inch	6 inch

Package (Assembly)

	Using	Change Request
Factory	No change(RIST)	
Package	No change (TO-247N)	
Dimensions	No change	
Marking	No change	
Tube	No change	

※RIST:ROHM INTEGRATED SYSTEMS (THAILAND) CO.,LTD.

Specification

	Using	Change Request
Datasheet (Electrical Characteristics)	Same	
Reliability Test	OK	OK

4. Affected Products

Please refer to PNList

5. Factory Overview

- Company Name: Lapis Semiconductor Co., Ltd. Miyazaki Plant
- Representative: Kazumasa Wakuno(President and CEO)
- Location: 727 Kihara, Kiyotake, Miyazaki City, Miyazaki Prefecture
- Date of establishment: October 1, 2008
- Capital: 300 million yen (wholly owned by ROHM Corporation)
- Business: Power Devices, MEMS, WL-CSP, etc.
- Number of employees: 686 (as of October 2020)

5. Factory Overview

PCN No.2222002

Assembly process

ROHM Electronics Dalian Co., Ltd.

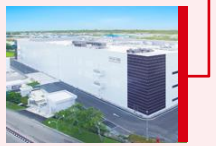
CIS PH S PM

ROHM Semiconductor (China)Co., Ltd

Di LED LD S DP

ROHM Korea Corporation

Tr Di SiC IGBT



ROHM-Wako Electronics (Malaysia)Sdn. Bhd.

Tr Di LED

ROHM Integrated Systems (Thailand) Co., Ltd.

IC Tr Di SiC IGBT IPM S R TC WM

ROHM Electronics Philippines, Inc.

IC S Tr Di R

Lapis Semiconductor Miyazaki Plant

IC S Di SiC IGBT

Front process (wafer manufacturing)

Lapis Semiconductor Miyagi Plant

IC

ROHM Hamamatsu (Shizuoka)

IC LED

Rohm Shiga Plant

Tr Di IGBT

Rohm Apollo (Fukuoka)

IC Tr Di SiC S TC

Rohm Wako (Okayama)

IC Di LED LD

Kyoto Head Office

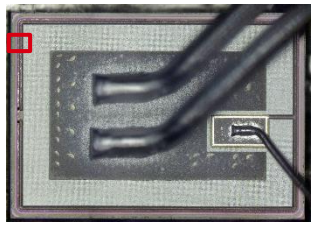
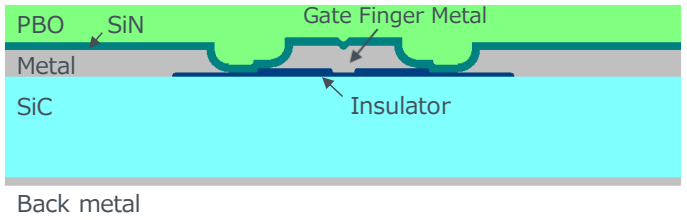
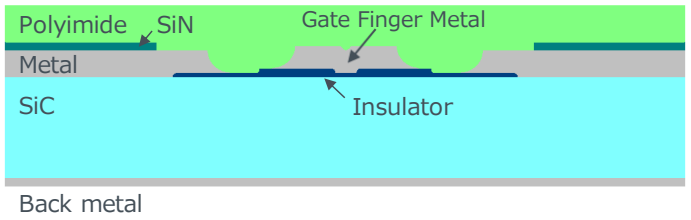
IC S Tr LED LD SiC

※ Wafer process is only part assembly process

6.List of changes

PCN No.2222002

■ List of changes from conventional products

Item	Current products	New products	Purpose of change
Factory	ROHM Apollo co., ltd. (Chikugo)	LAPIS Semiconductor Co., Ltd. (Miyazaki)	improve productivity
Wafer size	4inch	6inch	improve productivity
Back side metal	Ti-Ni(0.6μm)-Au-Ag Ti-Ni(1.2μm)-Au-Ag	Ti-Ni(1.2μm)-Au	improve productivity
Passivation	Polybenzoxazole (PBO)	Polyimide (PI)	improve productivity
Passivation structure of outer peripheral area (red frame below) 			improve against passivation cracks due to thermal stress

For 6inch products ,the back metal composition and passivation structure will change.

7.Comparison of production plants

		Conventional factory	Additional approval factory
Production plant		Rohm Apollo Chikugo	Lapis Semiconductor Miyazaki
Wafer Diameter		4inch,6inch,8inch	6inch
Clean room	Temperature	23℃	23℃
	Humidity	45%	45%
	Cleanliness* (wafer exposure area)	Class3(0.1um)	Class4(0.1um)
	Airflow method	laminar flow	laminar flow
Design Rules		0.35um	0.35um
Quality Management System		SPC System	SPC System

*Cleanliness is class according to ISO standards

There is no difference in The clean room environment of conventional factory and additional approval factory.

8.5M Change Point Verification

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		Target	Production plant		Concern	Verification	Decision
			current products	New products			
			Rohm Apollo Chikugo 4inch・6inch	Lapis Semiconductor Miyazaki 6inch			
Changes at **5M** level	Man	Operator	Adoption of licensing system	Adoption of licensing system	Difference in work skills	No skill difference	No problem
	Machine	Production equipment	6inch wafer-compatible equipment (4inch combined use)	6inch wafer-compatible equipment (Mass production results)	Difference in specification	Process change point verification Electrical characteristics Workmanship confirmation Reliability	No problem
	Material*	Wafer	4inch wafer	6inch wafer	Difference in specification, Reliability		
		Passivation	Polybenzoxazole	Polyimide			
		Back side metal	Ti/Ni/Au/Ag	Ti/Ni/Au			
	Method	Job method	6inch wafer process line (4inch combined use)	6inch wafer process line (Mass production results)	Difference in specification		
	Measurement	After wafer process measurement	6inch wafer-compatible equipment (4inch combined use)	6inch wafer-compatible equipment (Mass production results)	Difference in measurements between the provers	Correlation evaluation	No problem

*Materials are only those that have changed.

In accordance with the 5M change point, we confirmed that there are no problems.

9. Process Change Point Verification

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No	Process operation	Equipment and methods		material		Differences and concerns	Validation results	decision ○ or ×	document
		Apollo Chikugo	Lapis Miyazaki	Apollo Chikugo	Lapis Miyazaki				
1	Fab Input	-		4inch Wafer	6inch Wafer	Difference in inch diameter	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
2	Cleaning	Same type specifications		Same type chemicals		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
3	Oxidation	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
4	Photolithography (resist coating)	Same type specifications		Same type chemicals		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
5	Photolithography (exposure)	Same type specifications		-		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
6	Photolithography (resist development)	Same type specifications		Same type chemicals		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
7	Wet Etching	Same type specifications		Same type chemicals		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
8	Resist remove (ashing)	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
9	SiC Trench Etching (dry)	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
10	Implantation	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
11	Activation annealing	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24

We have confirmed that there are no problems with all the changes in each process.

9. Process Change Point Verification

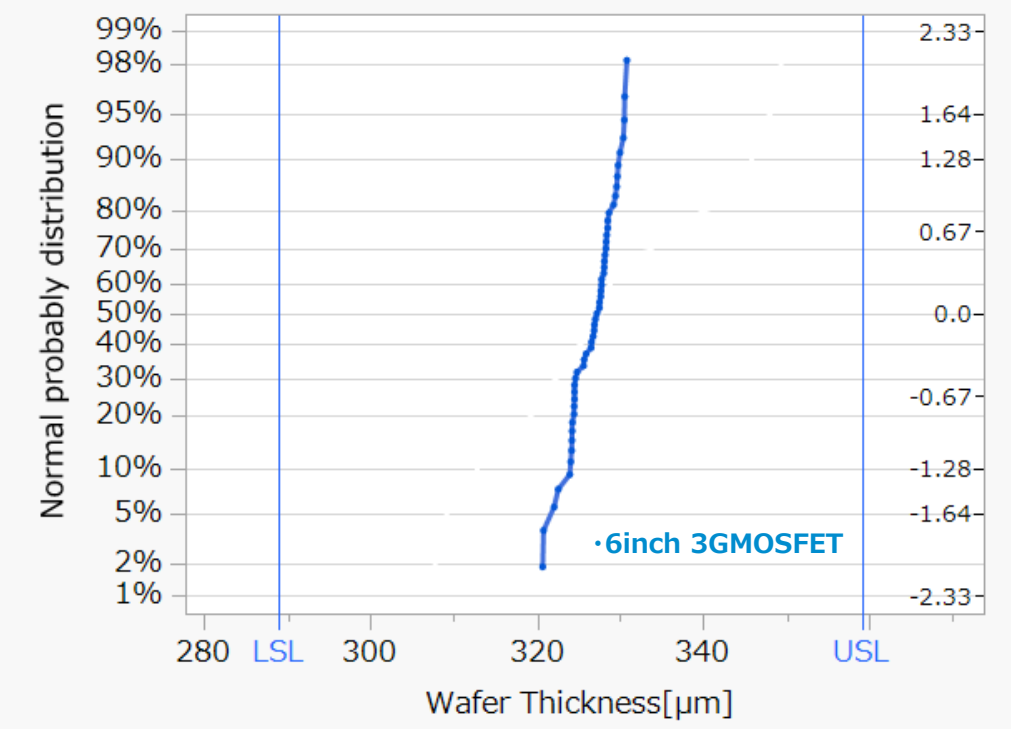
PCN No.2222002

No	Process operation	Equipment and methods		material		Differences and concerns	Validation results	decision ○ or ×	document
		Apollo Chikugo	Lapis Miyazaki	Apollo Chikugo	Lapis Miyazaki				
12	Formation of poly-Si	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
13	Poly-Si Etching (dry)	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
14	Deposition inter-layer	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
15	SiO2 interlayer Etching(dry)	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
16	Forming surface electrode	Same type specifications		Same type materials		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
17	Metal Etching (Wet)	Same type specifications		Same type chemicals		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
18	Metal Etching (Dry)	Same type specifications		Same type gas		Nothing	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
19	Forming passivation layer	Same type specifications		PBO	PI	Use different materials Reliability	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
20	Back Side Grinding	Done before Fab Input	New process	Same type materials		New process	No difference in Wafer thickness No difference in specification No failure in reliability test	○	P.14 P.15-17 P.18-24
21	Forming backside electrode	Same type specifications		Ti/Ni/Au/Ag	Ti/Ni/Au	Layer structure change Reliability	No difference in specification No failure in reliability test	○	P.15-17 P.18-24
22	Electrical characteristic test	Same type specifications		–		Nothing	No difference in specification	○	P.15-17
23	Dicing	Same type specifications		Same type materials		Nothing	No difference in specification	○	-

We have confirmed that there are no problems with all the changes in each process.

10. Product Performance Evaluation Results

■ SiC wafer thickness after Grind



*The graph on the left shows the thickness of only the board.
The wafer thickness described in the data sheet contains the thickness of the metal.

*USL: Upper Specification Limit
LSL: Lower Specification Limit

Wafer	6inch
Average	326.7µm
σ	2.5µm

We confirmed that there is no problem with the process capability of the grinding process(new process).

11. Summary of Evaluation Results

	4inch 3GMOSFET (Apollo Chikugo)	6inch 3GMOSFET (Lapis Miyazaki)
Static Characteristics (I_{DSS},I_{GSS},V_{th},V_{SD},R_{on})	Same Value	
Dynamic Characteristics (C_{iss},C_{oss},C_{rss},Q_g,Q_{gs},Q_{gd})	Same Value	
Switching Characteristics	Same Value	
Thermal Resistance	Same Value	
Electrical Static Discharge	Same Value	
Gate Oxide Reliability	Same Value*checked by TDDB test	
Reliability Test Result	AEC-Q101 qualified	AEC-Q101 qualified

There is no difference in various electrical characteristics between 4inch products and 6inch products.

12. Comparison of electrical characteristics

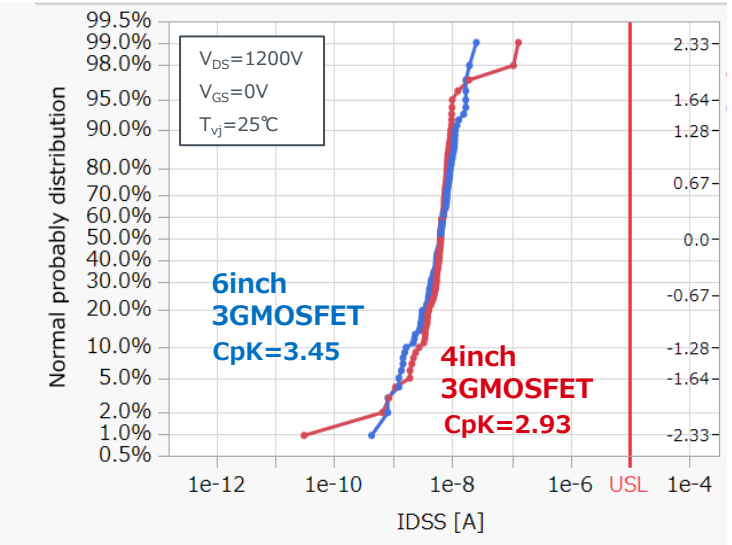
PCN No.2222002

■ Electrical Characteristics normal probability distribution (T_{vj}=25℃)

- **4inch 3GMOSFET [SCT3040KLHRC11]**
- **6inch 3GMOSFET [SCT3040KLHRC11]**

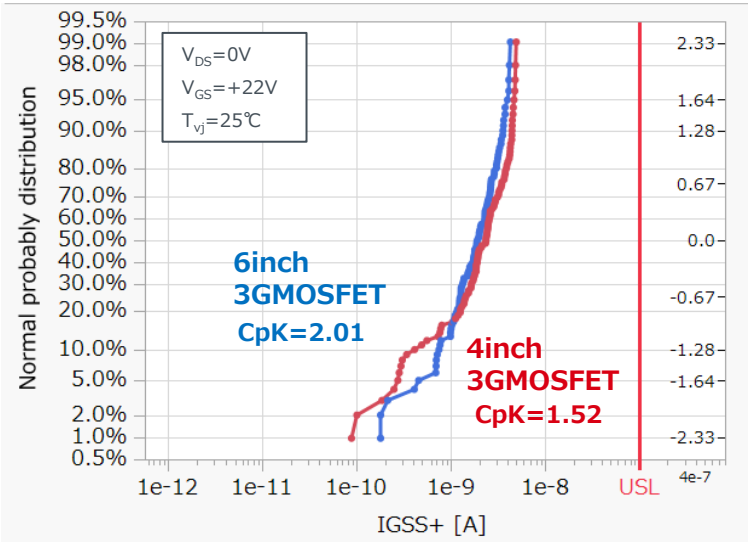
*USL: Upper Specification Limit
LSL: Lower Specification Limit

Zero Gate voltage Drain current [I_{DSS}]



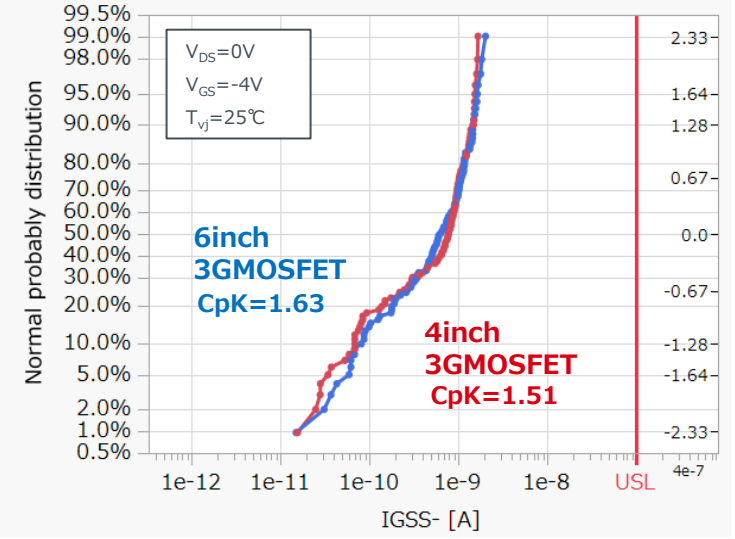
Wafer	N[pcs]	Ave[μA]	max[μA]	min[μA]	σ[μA]
4inch	100	0.00843	0.13011	0.00003	0.00679
6inch	100	0.00673	0.02534	0.00043	0.00430

Gate-Source leakage current [I_{GSS}(V_{GS}=22V)]



Wafer	N[pcs]	Ave[nA]	max[nA]	min[nA]	σ[nA]
4inch	100	2.394	4.919	0.087	1.353
6inch	100	2.031	4.263	0.178	1.006

Gate-Source leakage current [I_{GSS}(V_{GS}=-4V)]



Wafer	N[pcs]	Ave[nA]	max[nA]	min[nA]	σ[nA]
4inch	100	0.716	1.658	0.016	0.486
6inch	100	0.713	2.015	0.015	0.512

There is no difference in various electrical characteristics between 4inch products and 6inch products.

12. Comparison of electrical characteristics

PCN No.2222002

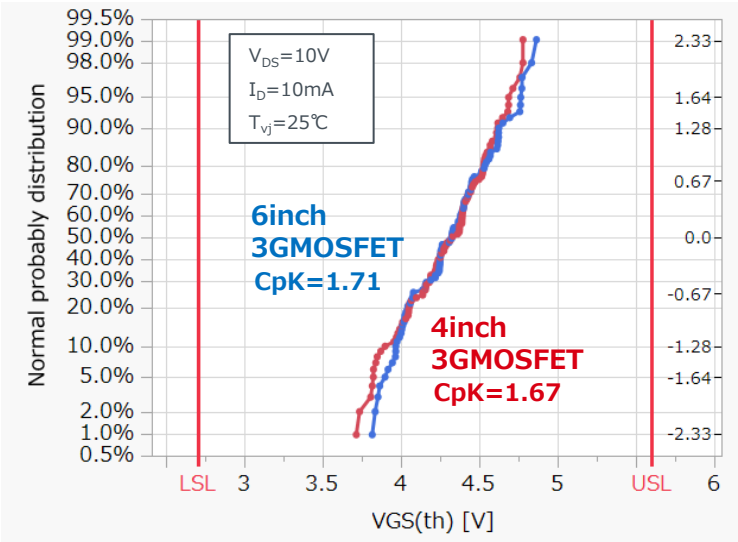
■ Electrical Characteristics normal probability distribution (T_{vj}=25℃)

・4inch 3GMOSFET [SCT3040KLHRC11]

・6inch 3GMOSFET [SCT3040KLHRC11]

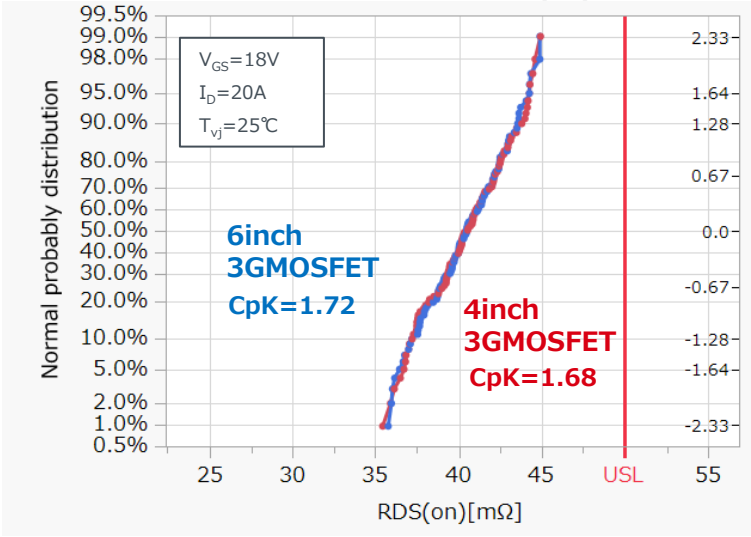
*USL: Upper Specification Limit
LSL: Lower Specification Limit

Gate threshold voltage [$V_{GS(th)}$]



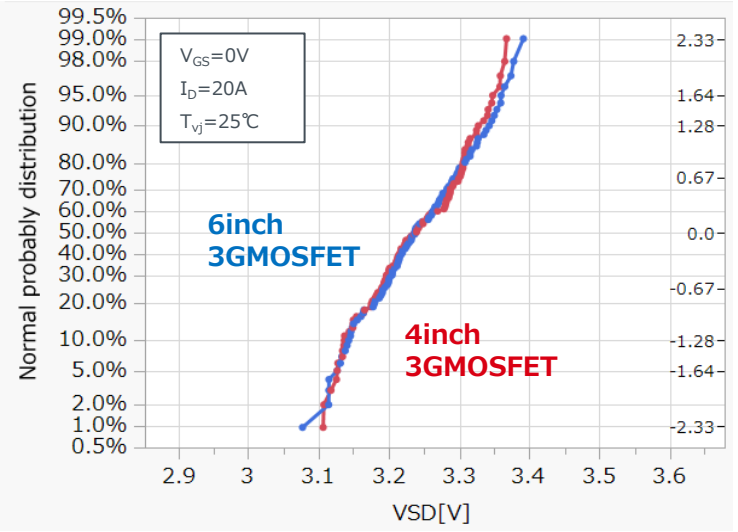
Wafer	N[pcs]	Ave[V]	max[V]	min[V]	σ[V]
4inch	100	4.30	4.78	3.72	0.26
6inch	100	4.31	4.87	3.82	0.25

Static Drain-Source on-state resistance [$R_{DS(on)}$]



Wafer	N[pcs]	Ave[mΩ]	max[mΩ]	min[mΩ]	σ[mΩ]
4inch	100	40.46	44.92	35.43	2.29
6inch	100	40.45	44.88	35.76	2.24

Forward voltage [V_{SD}]



Wafer	N[pcs]	Ave[V]	max[V]	min[V]	σ[V]
4inch	100	3.24	3.27	3.11	0.07
6inch	100	3.24	3.39	3.08	0.07

There is no difference in various electrical characteristics between 4inch products and 6inch products.

13. Reliability Test Results

PCN No.2222002

■ List of test results

Test items	Test conditions	Compliant standards	Exam time	Sample size n(pcs)	Failure Pn (pcs)
High Temperature Reverse Bias(HTRB)	T_a=175℃, V_{DS}=V_{DSmax}	AEC-Q101	1000 h	77×3lot	0
High Temperature Reverse Bias(HTGB+)	T_a=175℃, V_{GS}=V_{GSmax}	AEC-Q101	1000 h	77×3lot	0
High Temperature Reverse Bias(HTGB-)	T_a=175℃, V_{GS}=V_{GSmin}	AEC-Q101	1000 h	77×3lot	0
Temperature humidity bias(THB)	T_a=85℃, Rh=85%, V_{DS}=100V	AEC-Q101	1000 h	77×3lot	0
Temperature cycle (TCY)	T_a=-55℃(30min)～T_a=150℃(30min)	AEC-Q101	1000 cycles	77×3lot	0
Pressure cooker(AC)	T_a=121℃, 2atm, Rh=100%	AEC-Q101	96 h	77×3lot	0

※Pretreatment conditions: Aging with pressure-docker equipment (105°C, 100%, 1.22×105Pa, 4h)

■ Measurement items and failure criteria

Measurement items	Conditions	Failure criteria
Gate-Source leakage current(I_{GSS})	Depends on specification conditions	Complies with AEC-Q101 standards
Zero Gate voltage Drain current (I_{DSS})	Depends on specification conditions	Complies with AEC-Q101 standards
Gate threshold voltage ($V_{GS(th)}$)	Depends on specification conditions	Complies with AEC-Q101 standards
Static Drain-Source on-state resistance ($R_{DS(on)}$)	Depends on specification conditions	Complies with AEC-Q101 standards

As a result of the reliability test, it was confirmed that there was no problem.

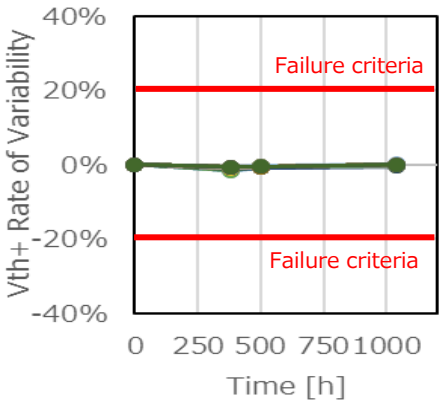
13. Reliability Test Results (HTRB)

PCN No.2222002

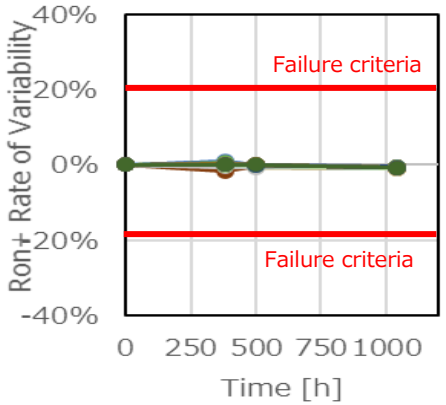
■ High Temperature Reverse Bias (HTRB) [V_{DS}=V_{DSmax}, T_a=175℃]

Wafer:S4101MUFCZ
Package:SCT3040KL(TO-247N)
Sample size:77pcs×3lot

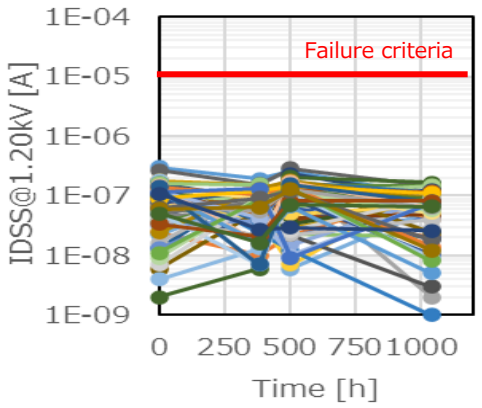
$V_{GS(th)}$ @I_{ds}=10mA



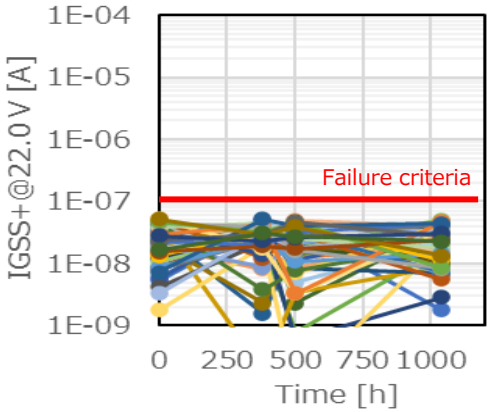
$R_{DS(on)}$ @I_{ds}=20A



I_{DSS} @V_{DS}=1200V



I_{GSS} @V_{GS}=22V



No Failure after 1000h over

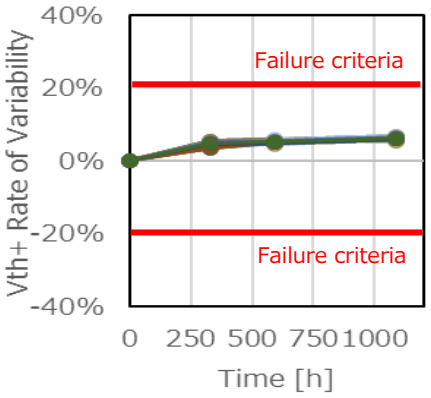
13. Reliability Test Results (HTGB)

PCN No.2222002

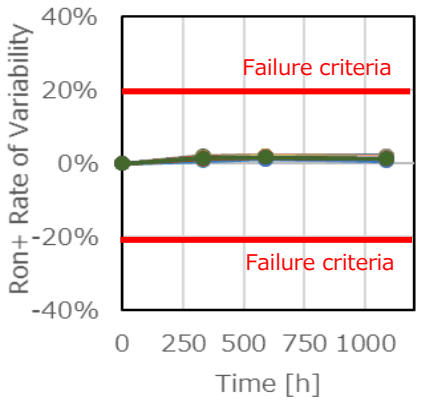
■ High Temperature Gate Bias+ (HTGB+) [$V_{GS}=V_{GSmax}$, $T_a=175℃$]

Wafer:S4101MUFCZ
Package:SCT3040KL(TO-247N)
Sample size:77pcs×3lot

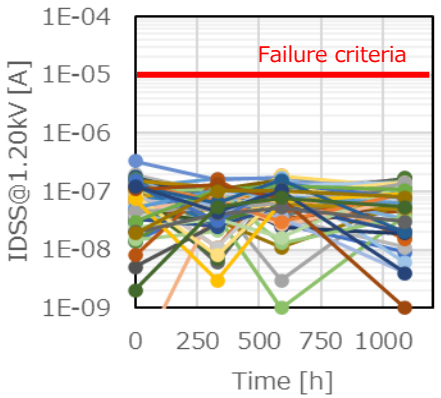
$V_{GS(th)}$ @I_{ds}=10mA



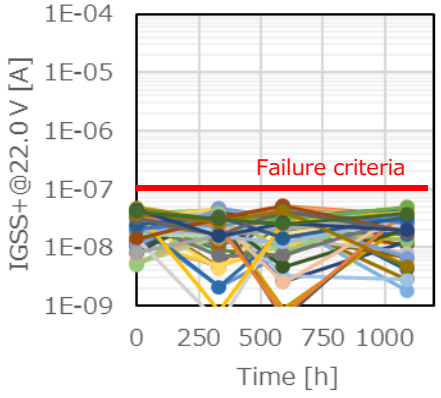
$R_{DS(on)}$ @I_{ds}=20A



I_{DSS} @V_{DS}=1200V

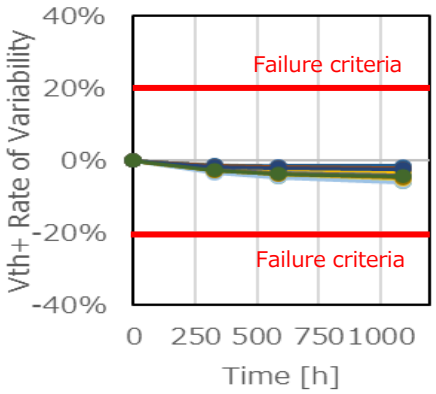


I_{GSS} @V_{GS}=22V

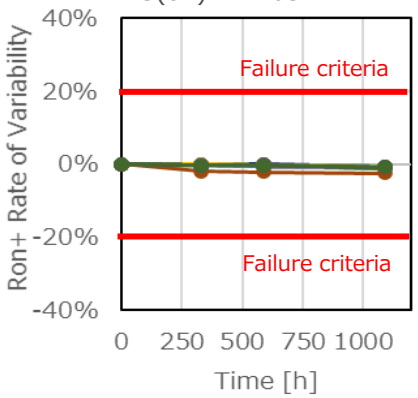


■ High Temperature Gate Bias- (HTGB-) [$V_{GS}=V_{GSmin}$, $T_a=175℃$]

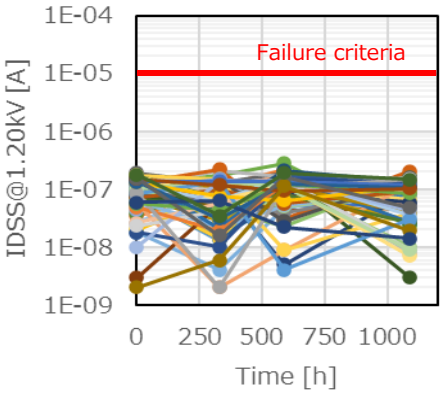
$V_{GS(th)}$ @I_{ds}=10mA



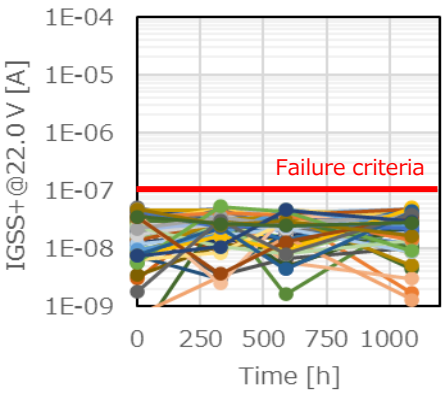
$R_{DS(on)}$ @I_{ds}=20A



I_{DSS} @V_{DS}=1200V



I_{GSS} @V_{GS}=22V



No Failure after 1000h over

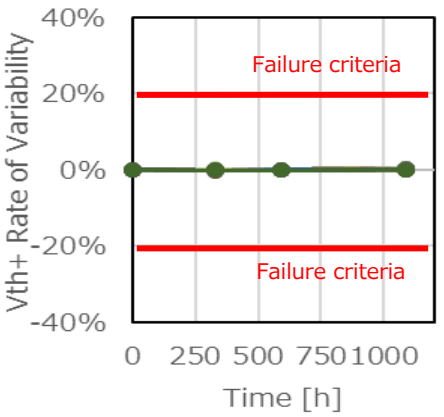
13. Reliability Test Results (THB)

PCN No.2222002

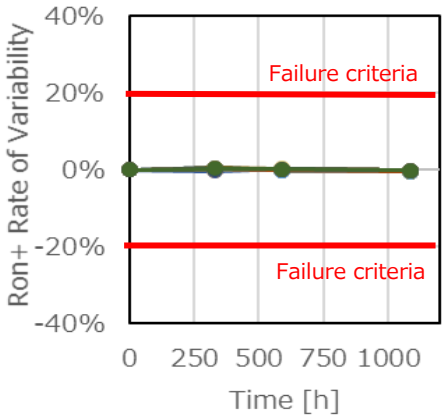
■ Temperature humidity bias(THB) [V_{DS}=100V, T_a=85℃, Rh=85%]

Wafer:S4101MUFCZ
Package:SCT3040KL(TO-247N)
Sample size:77pcs×3lot

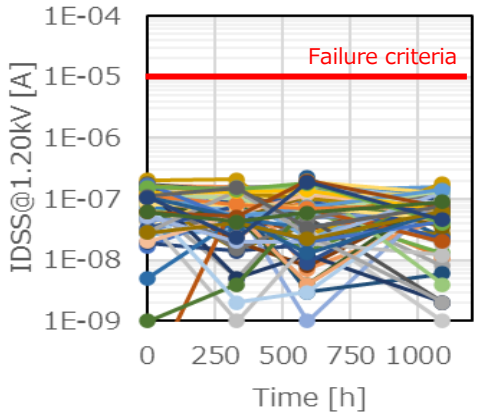
$V_{GS(th)}$ @I_{ds}=10mA



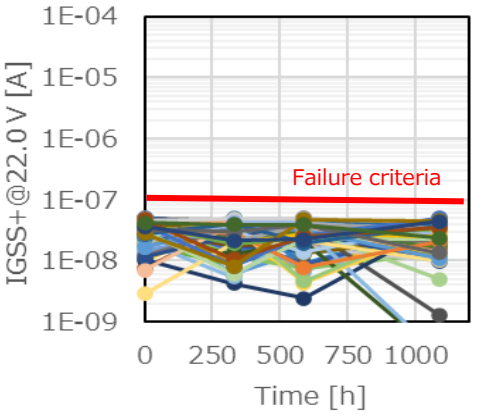
$R_{DS(on)}$ @I_{ds}=20A



I_{DSS} @V_{DS}=1200V



I_{GSS} @V_{GS}=22V



No Failure after 1000h over

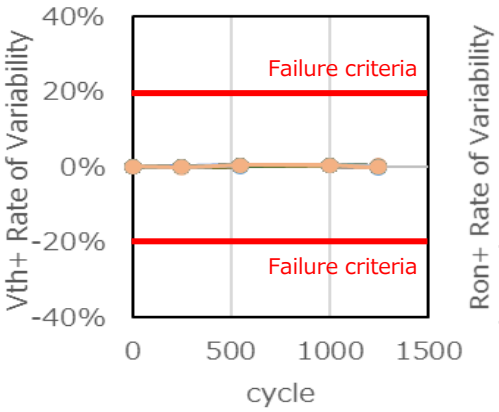
13. Reliability Test Results (TC)

PCN No.2222002

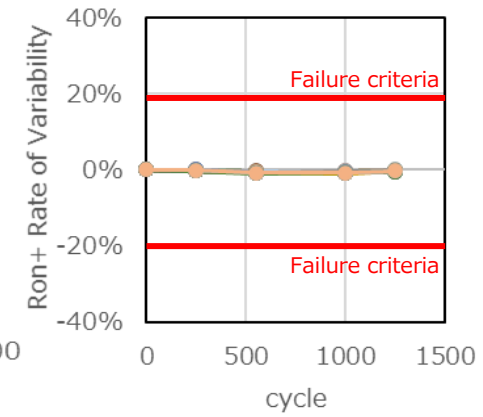
■ Temperature cycle (TC) [T_a=-55℃(30min)～150℃(30min)]

Wafer:S4101MUFCZ
Package:SCT3040KL(TO-247N)
Sample size:77pcs×3lot

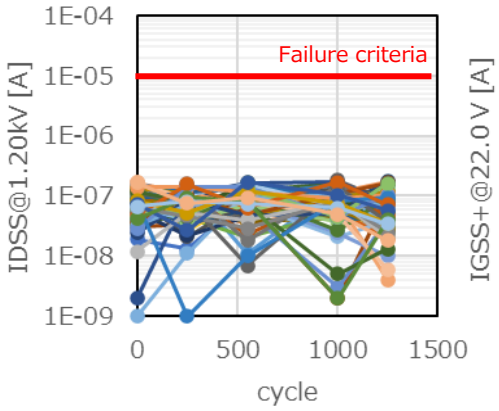
$V_{GS(th)}$ @I_{ds}=10mA



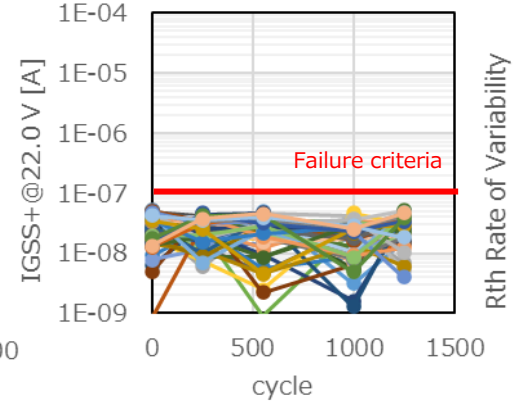
$R_{DS(on)}$ @I_{ds}=20A



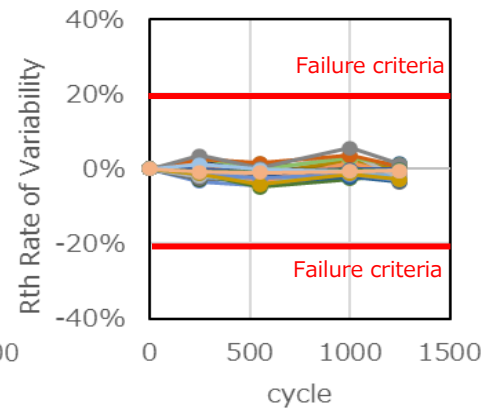
I_{DSS} @V_{DS}=1200V



I_{GSS} @V_{GS}=22V



Rth



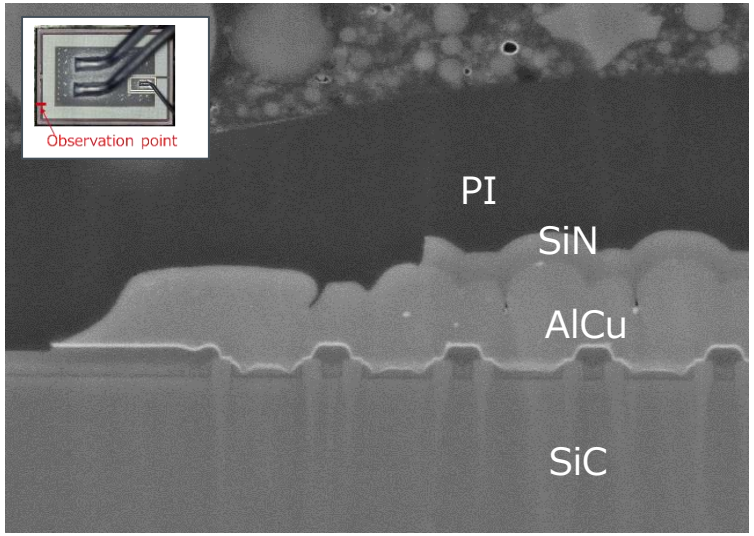
No Failure after 1000cycle over

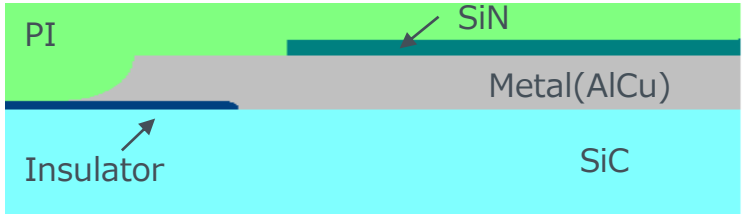
7-3. Reliability Test Results (TC)

PCN No.2222002

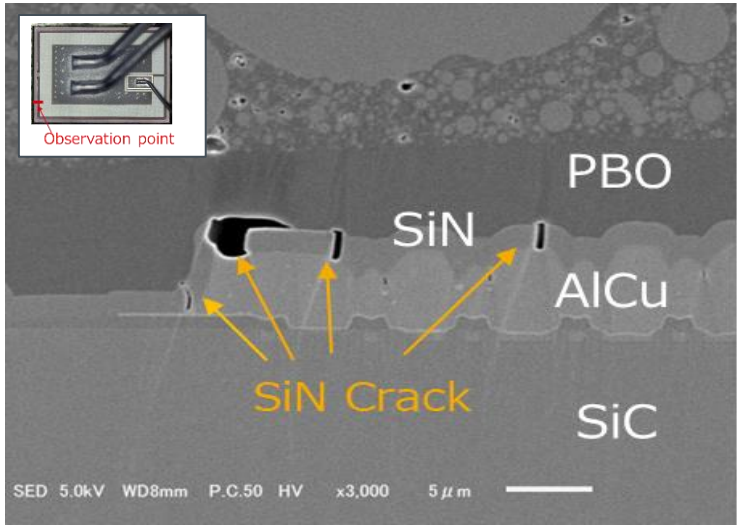
■ Cross sectional observation of Non-defective samples after TC 1000cyc

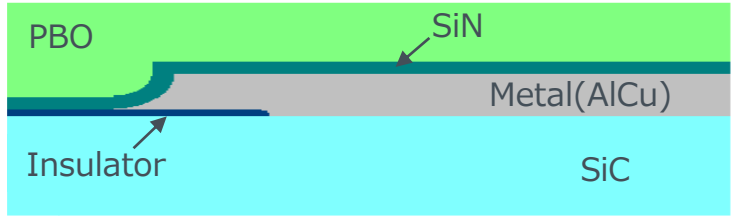
6inch 3GMOSFET [SCT3040KLHRC11]

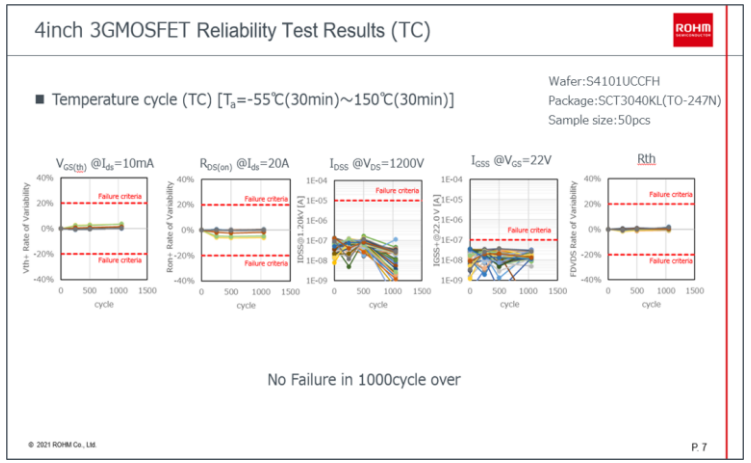




4inch 3GMOSFET [SCT3040KLHRC11]







In 4inch 3GMOSFET, SiN layer in outer peripheral area may be cracked due to thermal stress such as temperature cycles. However, at the time of the TC 1050 cycle, the cracks are minor and there are no changes in characteristics, so there is no problem.

Structural changes have improved robustness against the cracking of the passivation layer(SiN).

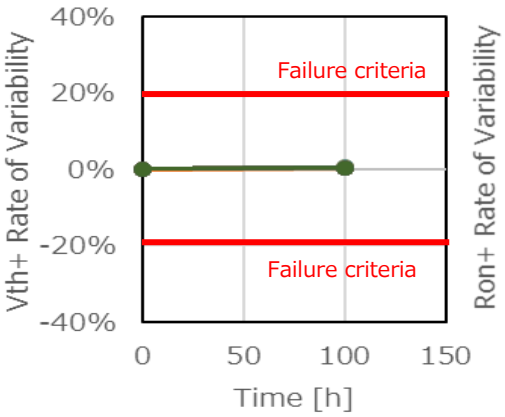
13. Reliability Test Results (AC)

PCN No.2222002

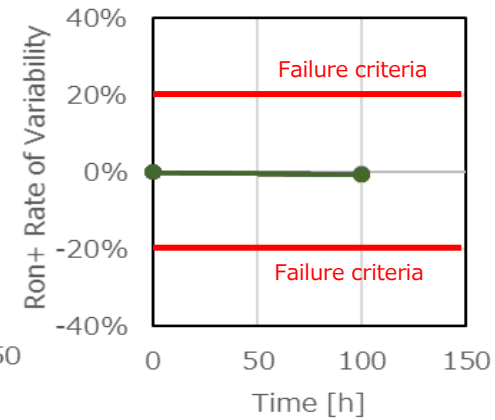
■ Pressure cooker (AC) [T_a=121℃, 2atm, Rh=100%]

Wafer:S4101MUFCZ
Package:SCT3040KL(TO-247N)
Sample size:77pcs×3lot

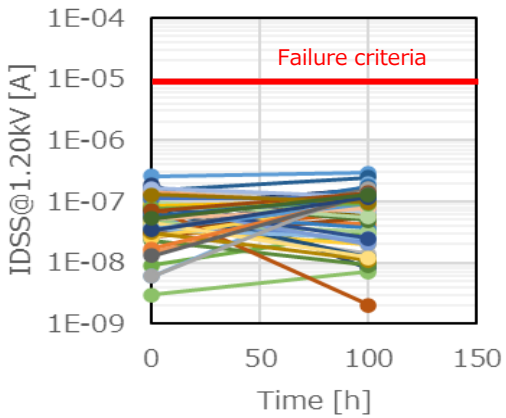
$V_{GS(th)}$ @I_{ds}=10mA



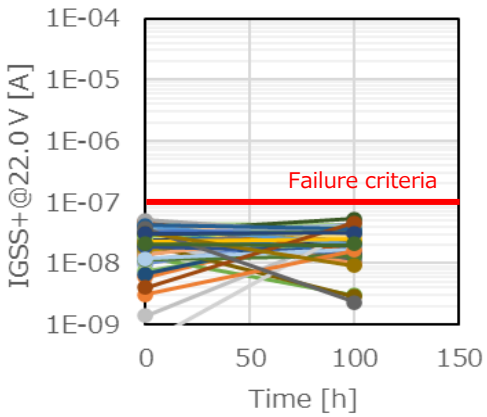
$R_{DS(on)}$ @I_{ds}=20A



I_{DSS} @V_{DS}=1200V



I_{GSS} @V_{GS}=22V



No Failure after 96h over

Electronics for the Future

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